From Semiconductor PPA Optimization to Physical AI: Library-Based Design Challenges and New Frontiers

November 12, 2025

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Introduction to Speaker

Carrer Evolution

Academia | Startup | Global Company

1997 2002 2005 2009 2012 2014 2015 2018 2021 2023 2024 2025

Seoul National University
Professor & Associate Dean

Korea Advanced Institute of Science and Technology (KAIST)
Professor & Associate Dean

Samsung SDI (battery) Korea (HQ)
Advisor → EVP/ Head of Development

Samsung SDI America
EVP

Samsung Electronics Device Solutions America
Full-time Advisor

Sindo Ricoh Co. Ltd.
Multifunction printers
Technical advisor

EMVcon Inc. @California
Mobility electrification
Founder, CEO & Chairman

Axion Co. Ltd.
AI-based standard cell library optimization
Technical advisory board member

Arizona State University
Visiting Professor

University of Southern California
Visiting Professor

IEEE Fellow

ACM Fellow

National Academy of Engineering of Korea

Research Contributions

- Cross-Domain Research
- Low-power systems
- Design Automation of Things (DAoT)

Collaborative Research*

Cross-Cutting CSE Research

- Technical Excellence
- H-Index of 50, 8300+ Google Citations
- ACM/IEEE Fellow, NAEK member

- University of Southern California, Arizona State University, Penn State University, Carnegie Mellon University, Tsinghua University, Politecnico di Torino, Technical University of Munich, National Taiwan University, Hong Kong Poly University, etc.
- Stellantis (previously known as Fiat Chrysler), General Motors, Audi, VWG, BMW, Volvo AB, Hyundai, Rivian, etc.

ACM Special Interest Group on Design Automation (SIGDA) Chair
53rd ACM/IEEE Design Automation Conference Program Chair
Editor-in-Chief of ACM Transactions of Design Automation of Electronic Systems

Introduction to Speaker

Technical Excellence

Circuits and Systems Design

- Digital, analog, mixed-signal, and high-voltage circuits
- High-power electronic circuits and systems
- High-precision and high-voltage circuit design
- VLSI (Very-Large-Scale Integration) design
- Power electronics devices and systems
- Data conversion: analog-to-digital (ADC) and digital-to-analog (DAC)

Embedded Systems and Programmable Devices

- Programmable Logic Controllers (PLC)
- Programmable logic devices and FPGAs (Field-Programmable Gate Arrays)
- System-level integration with various sensor and actuator interfaces
- Diverse I/O interface circuit design

Power and Thermal Management

- Power conversion: AC–DC and DC–DC systems
- PCB design with emphasis on signal and power integrity
- Delay, power, and thermal analysis
- Active and passive thermal management techniques

Design Automation and Toolchains

- Electronic Design Automation (EDA) methodologies and tools
- Cross-domain optimization for power, performance, and cost

Battery Technology and Energy Storage

- Battery chemistry, electrode design, and cell formats
- Current collector design and manufacturing process insight
- Battery characteristics, testing methodologies, and lifetime modeling
- Battery safety across cell, module, pack, and system levels
- Battery module and pack architecture
- Battery Management Systems (BMS): hardware, software, and safety integration
- Grid-scale energy storage systems and solar integration strategies

Renewable Energy Systems

- Photovoltaic (solar) cell array systems and thermoelectric generators (TEGs)
- Maximum Power Point Tracking (MPPT) for solar and hybrid energy sources

Electric Vehicles and Electrification Architecture

- Electric powertrain systems: high-voltage battery packs, onboard chargers, and HV–LV converters
- Vehicle system architecture, including chassis, steering, suspension, braking, and propulsion systems
- Electrical Control Units (ECUs), CAN communication protocols, and vehicle integration

Architecture and Systems Integration

- Computer architecture
- Microprocessor, memory, I/O, communication, and system-level integration
- Memory system architecture
- Embedded systems and the Internet of Things (IoT)
- Distributed systems
- Low-power computer design
- System software and cybersecurity

Control, Real-Time, and Embedded Systems

- Real-time control and monitoring systems
- Embedded programming and real-time operating systems (RTOS)
- Real-time systems development
- Dynamic power and thermal management
- Embedded and real-time system optimization

Algorithms and Intelligence

- Algorithms, modeling, and system-level optimization
- AI/ML techniques applied to systems and electronics
- Dynamic system adaptation through predictive and data-driven methods

Software & Interfaces

- Computer graphics: hardware and software
- Communication networks and protocol stacks
- Real-time and embedded OS-level software development

AI Semiconductor Areas

- Integrated circuits designed to accelerate artificial intelligence workloads such as training, inference, and data analytics
- Also include the use of AI to design and optimize chips: a bidirectional relationship between **AI for Chips** and **Chips for AI**

Chips for AI (Hardware Acceleration Domain)

- Hardware platforms purpose-built to execute AI algorithms efficiently
- Compute Engines: GPU, NPU, TPU, FPGA, ASIC accelerators
- Memory Subsystems: HBM, LPDDR5, on-chip SRAM, cache hierarchies
- Interconnects: NVLink, PCIe Gen5/6, CXL, chiplet fabrics
- Edge AI Processors: Low-power SoCs for mobile, automotive, robotics, and IoT inference
- System Integration: 2.5D/3D IC, chiplet-based heterogeneous architectures

AI for Chips (AI-Driven Semiconductor Design)

- Applying AI and machine learning to automate and enhance semiconductor development.
- Architecture Search & Design Space Exploration
- Logic Synthesis and Timing Optimization
- Floorplanning, Placement & Routing (P&R)
- DRC/LVS/Verification Automation
- EDA Workflow Optimization (Reinforcement Learning, GNN, LLM Integration)

AI Semiconductor Areas

- Extended Scope

System-Level Integration

- AI semiconductors extend beyond the chip to include AI-optimized system design
- AI-driven thermal, power, and packaging co-design
- Co-optimization of hardware, firmware, and control algorithms
- Digital twin–based validation and predictive optimization

Physical AI and Domain Convergence

- Bridging control, systems, and AI domains through physical-world intelligence
- Pretrained domain-knowledge libraries enabling embedded AI at the system level
- Integration of reinforcement learning and MPC controllers for adaptive physical systems

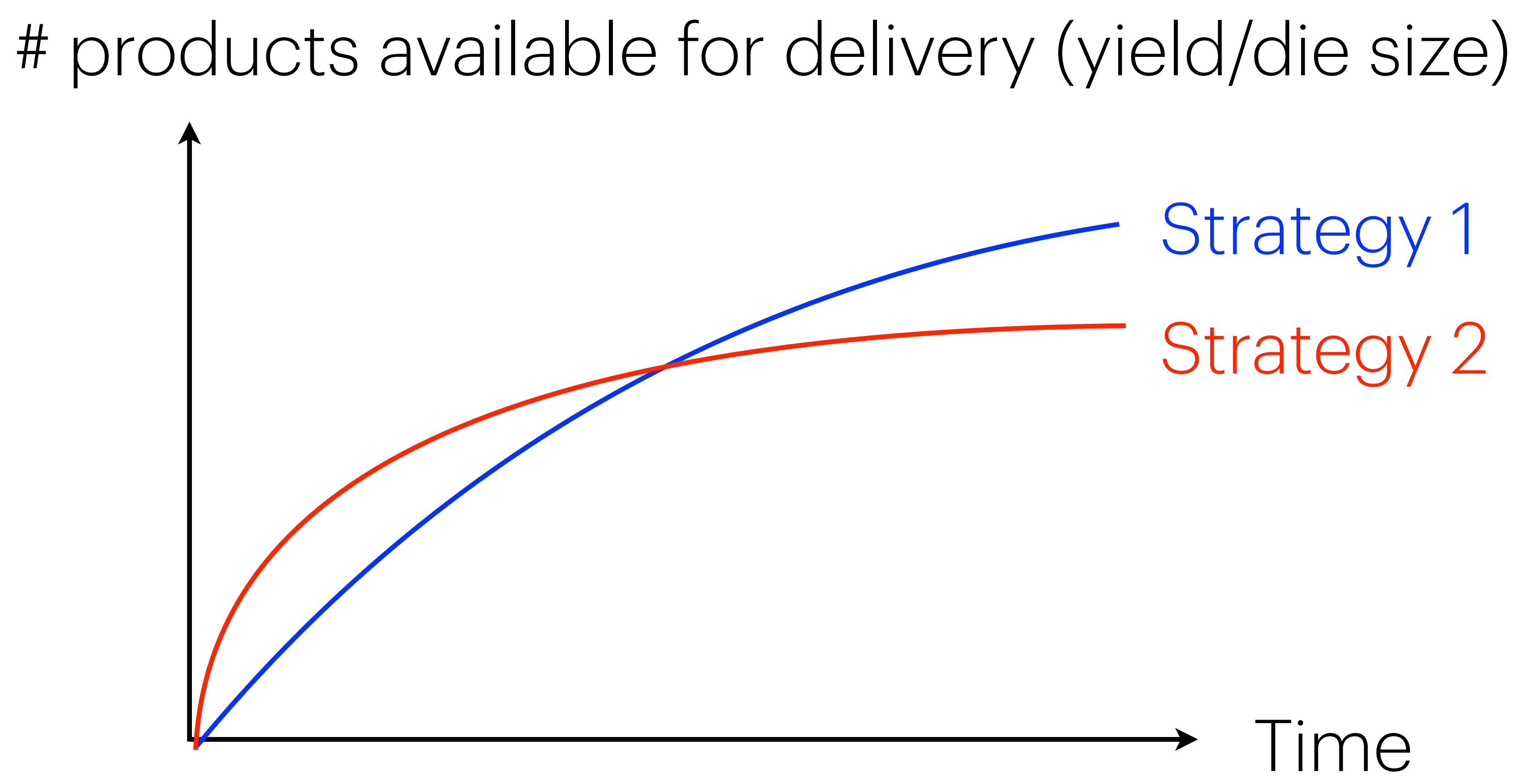
AI Semiconductor Areas

- Chips for Physical AI in market
  - NVIDIA Jetson/IGX: GPU + DLAs + vision accelerators; rich I/O for robotics/industrial edge
  - STM32N6 (MCU with NPU): integrates an on-chip NPU for edge AI with MCU-class control/I/O
  - Syntiant NDP: always-on sensor/audio AI at microwatts for wearables/IoT
  - Hailo-8/10: add-on edge AI accelerators for embedded systems
  - Ambarella CV3: automotive AI domain controller SoC (AI + ISP + I/O) used in autonomy stacks
  - Tesla FSD: custom automotive AI SoC with high-rate camera ingest and video pipeline
  - BrainChip Akida: neuromorphic edge inference with event-based sensors/on-chip learning

- AI semiconductors are central to: PPA (Power–Performance–Area) optimization under AI workload constraints
  - Energy-efficient AI scaling from cloud to edge
  - Sustainable technology migration across nodes (5 nm → 3 nm → 2 nm)
  - Next-generation Physical AI systems integrating sensing, control, and learning
  - How do we define PPA for Physical AI chips?

Library-Based Design

- Builds complex systems using pre-verified, reusable building blocks (libraries) instead of starting from scratch
- In semiconductors, libraries include standard cells, IP blocks, analog macros, and layout generators qualified by foundries or EDA vendors
- Each library element encapsulates domain knowledge, design rules, and performance characterization
- Designers focus on system integration and optimization, while the libraries ensure functional and physical correctness
- The process scales from RTL synthesis → layout → verification → sign-off, drastically shortening development cycles
- Key advantages in
  - Design Time
  - Verification
  - Engineer Productivity
  - Business Alignment
  - Design Reuse
  - Technology Migration
  - Cross-Domain Application
- The same concept now extends to robotics, AI, control, and energy systems, where reusable digital or physical modules accelerate innovation



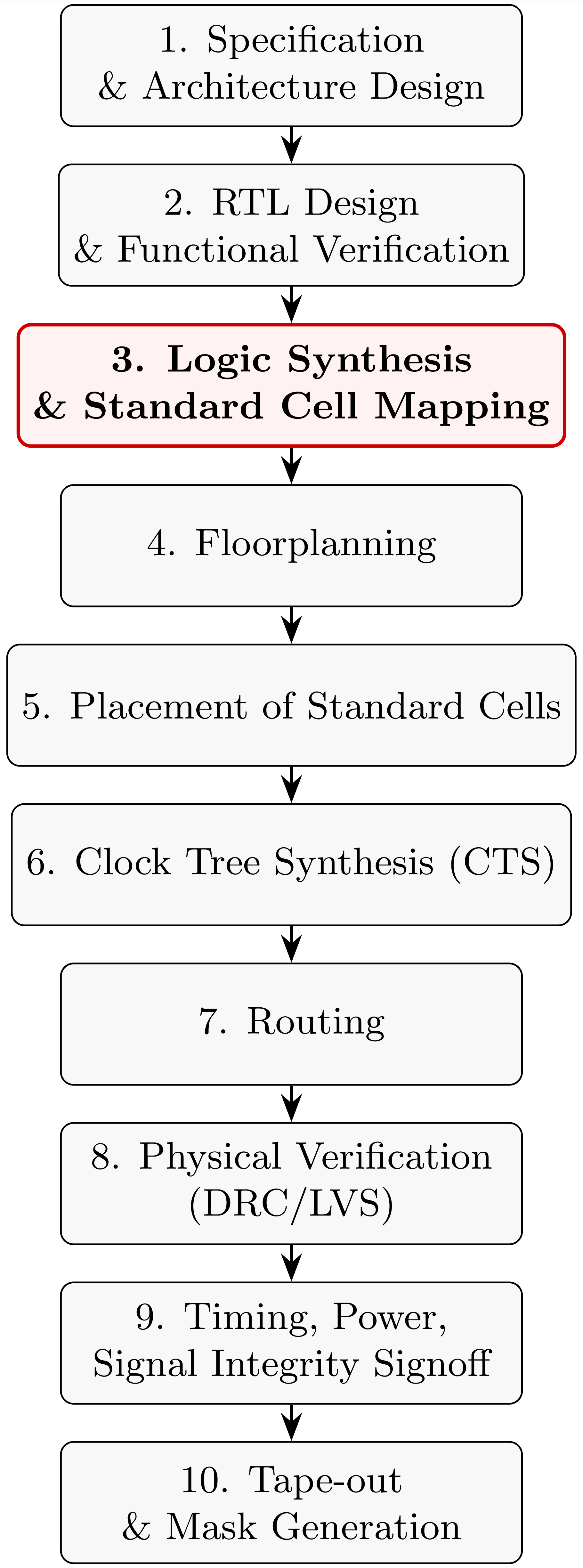
Time-to-market leadership

Introduction to Axion

- Axion Co. Ltd. (www.axion-technologies.com)
  - Founded in March 2024, currently based in Korea, with plans to expand business and development operations in the United States
  - Founder: Dr. Kee-Sup Kim
    - 8 years at Synopsys as Chief Technology Officer (CTO): Strategic collaboration, technology sensing, and growth strategy development
    - 4 years at Samsung Electronics as Vice President: Establishment of design methodologies and infrastructure
    - 17 years at Intel as Director of DFX (Intel Communications Group): Responsible for structural and functional test optimization for Intel CPUs
    - Honors and awards
      - IEEE A. Richard Newton Technical Impact Award
      - IEEE Don O. Pederson Award (X-Compact)
      - Intel Achievement Award
      - Ministry of Commerce (Republic of Korea) Green Technology Award
      - Multiple Samsung System LSI President's Awards
- Products
  - Axion Cell
  - Axion DFM
  - Axion Axion X
- My role as Technical Advisor
  - Strategic extension from Axion Cell to Axion X
  - To build and sustain a collaborative culture that achieves genuine, chemistry-level integration between Electrical Engineering and Computer Science

Standard Cells

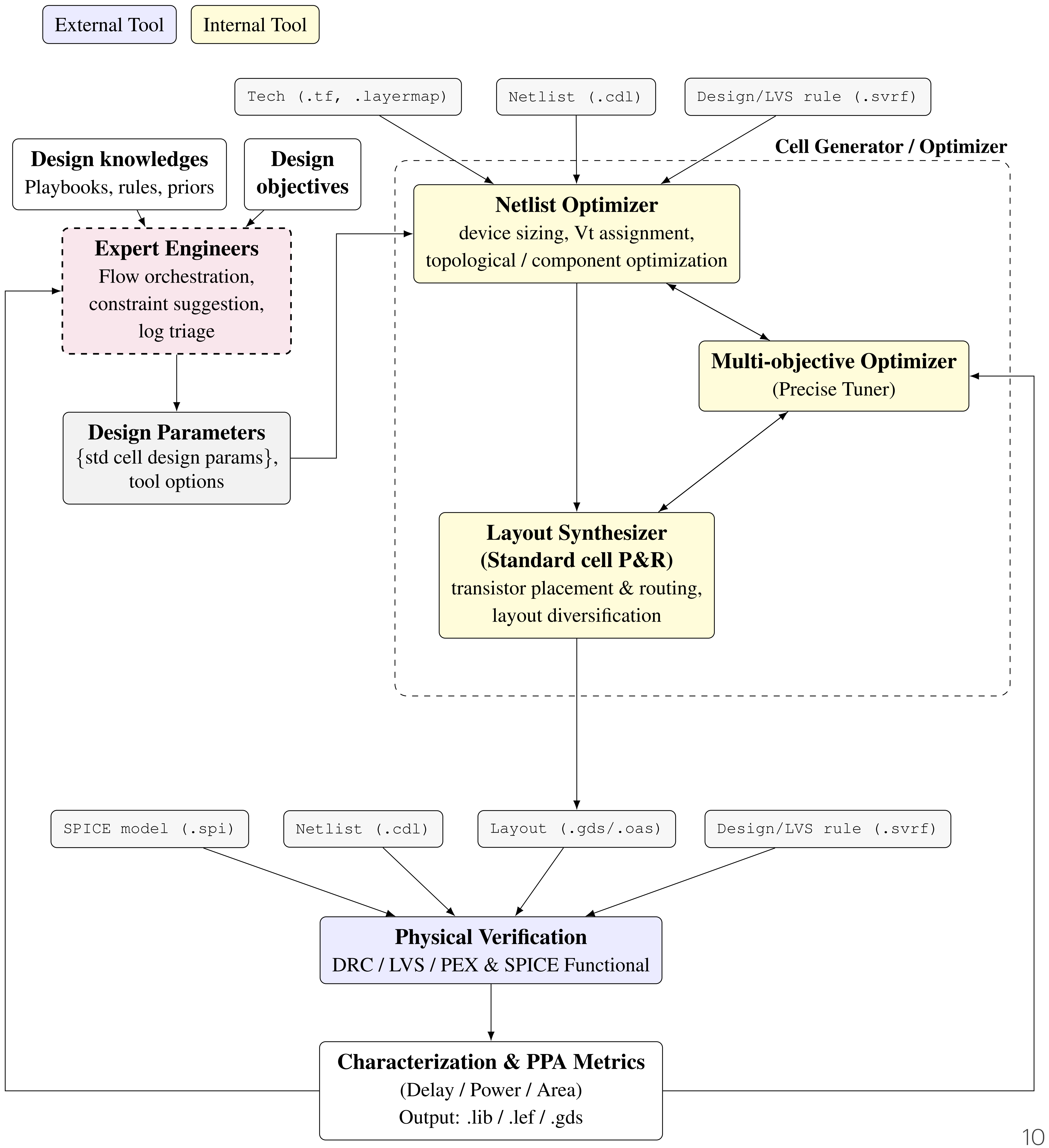
- A pre-designed, pre-characterized logic block that implements a basic digital function
  - Euch as NAND, NOR, XOR, inverter, flip-flop, or latch
  - Logical behavior (described in a Liberty .lib file)
  - Physical layout (in LEF/GDS format)
  - Timing, power, and area data characterized for different process-voltage-temperature (PVT) corners
  - Standard cells are designed and verified by library vendors or foundries (e.g., TSMC, Samsung, GF), and they form the reusable foundation for ASIC and SoC design
- Advantages of standard cells
  - Reusability: Eliminates the need to design transistors manually
  - Automation: Enables full digital design automation using EDA tools
  - Predictability: Each cell's timing and power are pre-characterized, allowing accurate optimization
  - Scalability: Libraries can be updated for new process nodes (e.g., 5nm → 3nm)
- Standard cell optimization still has headrooms to optimize
  - Lack of automation
  - Lack of time and efforts



Axion Cell Optimization

- Goal
  - Automate standard-cell optimization from netlist to layout
  - Achieving low-power or high-performance cells through multi-objective tuning

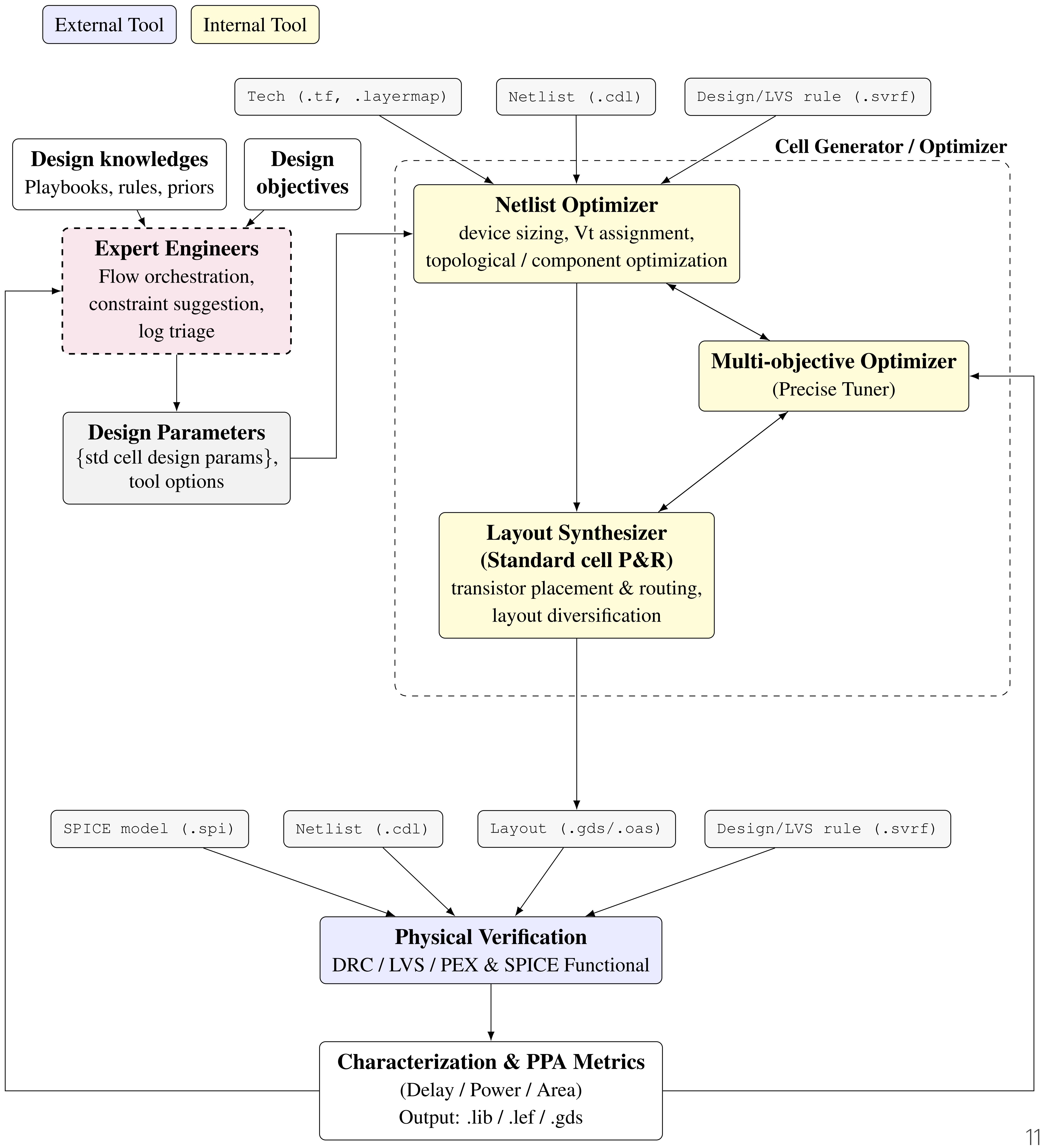
1. Design Knowledge & Parameters
   - Encode expert design insights for tuning key parameters
   - Parameters: track count, drive strength, VDD, Vth
   - Objectives: delay/performance or power efficiency
2. Netlist Optimizer
   - Input: netlist + tech file
   - Performs device sizing, topological optimization, and component substitution (e.g., tri-gate / transmission-gate)
   - Reduces area, leakage, and wirelength for better PPA
3. Layout Optimizer (Synthesizer)
   - Input: netlist + tech/design-rule files
   - Includes placer (diffusion sharing, wirelength & routability optimization) and router (metal/via reduction, pin accessibility)
   - Outputs layout (.gds)



Axion Cell Optimization

- Goal
  - Automate standard-cell optimization from netlist to layout
  - Achieving low-power or high-performance cells through multi-objective tuning

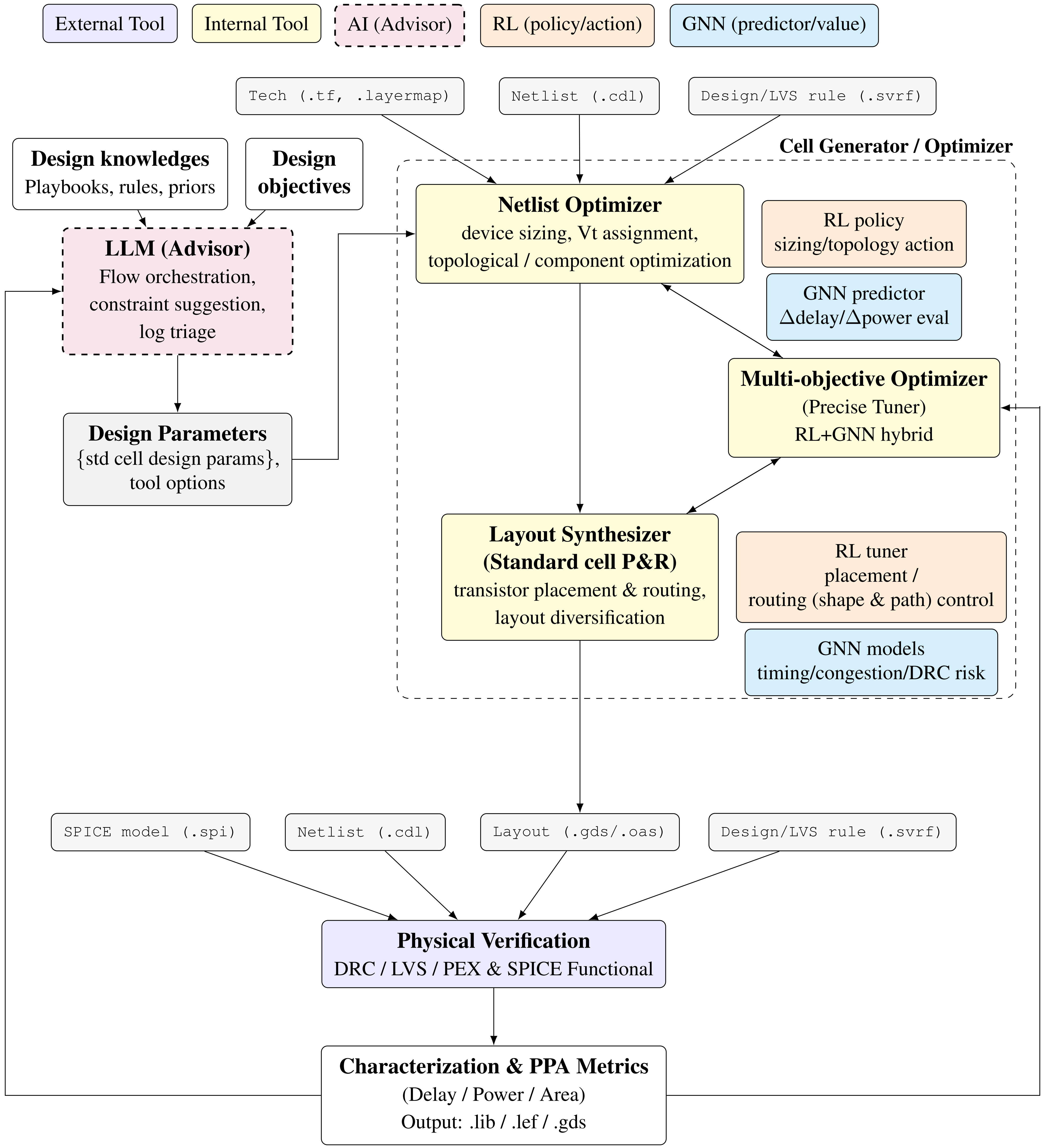
4. Multi-Objective Optimizer
   - Iteratively tunes parameters in netlist/layout stages
   - Balances power, performance, and area (PPA) trade-offs
5. Verification & Characterization
   - DRC/LVS → PEX (RC extraction) → SPICE simulation → Liberty (.lib)
   - Ensures functional correctness and generates final timing/ power models



AI-based Standard Cell Optimization

- Goal
  - Integrate AI-driven intelligence (LLM + RL + GNN) into the standard-cell optimization pipeline
  - Achieve autonomous optimization across netlist, layout, and verification stages for higher PPA and faster technology migration

1. AI Advisor (LLM)
   - Acts as knowledge-based orchestrator using design playbooks, rules, and priors
   - Performs flow orchestration, constraint suggestion, and log triage
   - Translates design intent → parameter guidance for downstream optimizers
2. RL-Driven Netlist Optimizer
   - RL agent controls sizing, Vt assignment, and topological/component transformations
   - Policy trained for PPA reward using feedback from GNN and SPICE simulations
   - Enables adaptive exploration beyond rule-based optimization
3. RL + GNN Hybrid Multi-Objective Optimizer
   - Combines RL action tuning with GNN-based evaluation (Δdelay, Δpower, DRC risk)
   - Guides parameter adjustment across netlist ↔ layout domains
   - Achieves balanced optimization for power, performance, and area



AI-based Standard Cell Optimization

- Goal
  - Integrate AI-driven intelligence (LLM + RL + GNN) into the standard-cell optimization pipeline
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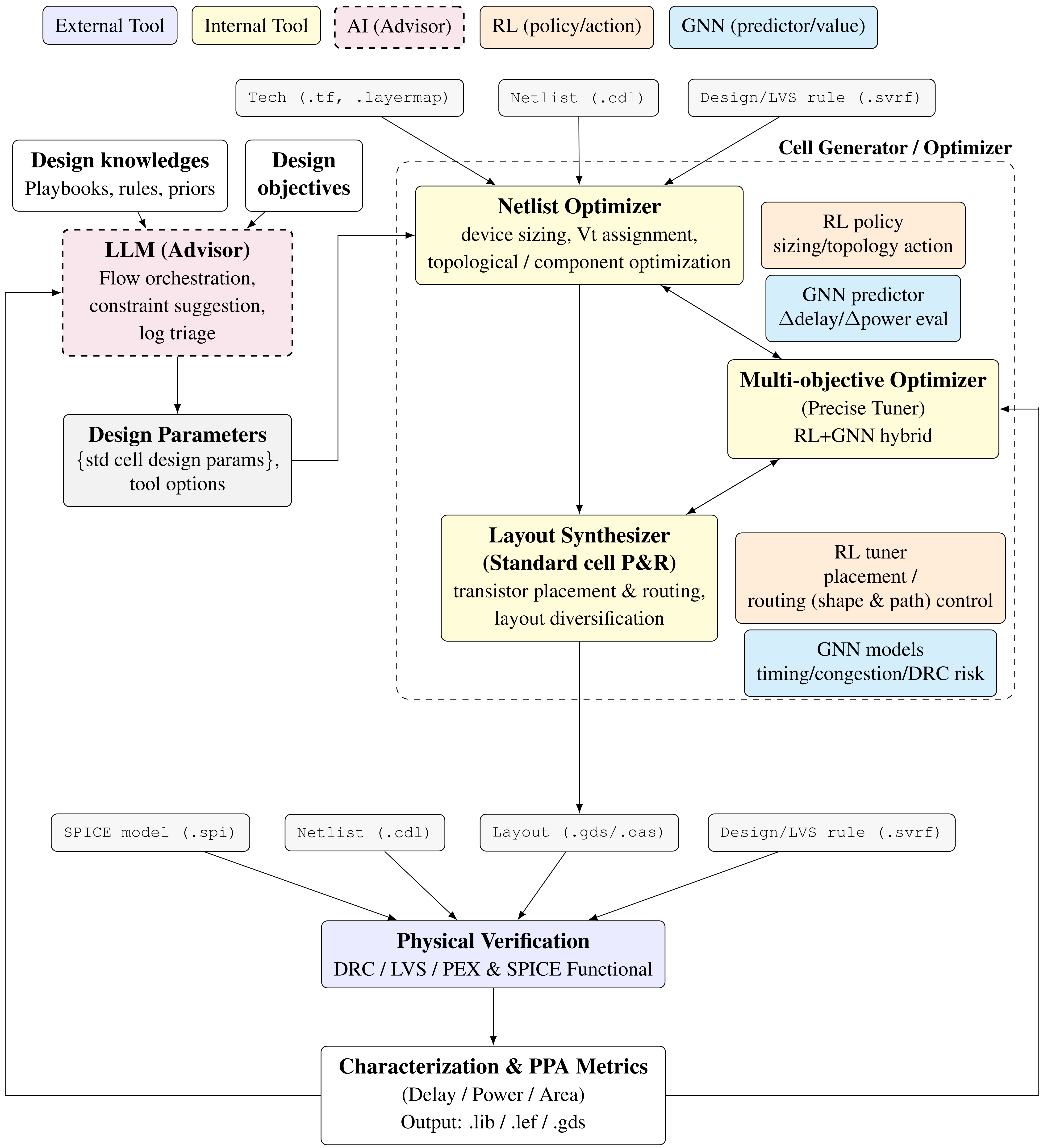
4. GNN-Enhanced Layout Synthesizer
   - Uses GNN predictors for routing congestion, timing, and DRC risk estimation
   - RL tuner controls placement and routing paths for routability and wirelength efficiency
   - Supports layout diversification and pin accessibility improvement
5. Verification & Characterization
   - Automated pipeline for DRC/LVS/PEX and SPICE functional validation
   - Generates Liberty (.lib), LEF (.lef), and GDS (.gds) models with AI-refined characterization

Outcome

- Continuous learning loop: LLM knowledge ↔ RL policy ↔ GNN predictor
- Enables self-improving cell generation, rapid PPA closure, and scalable tech migration



Physical AI Domain Definition

Axion X for Physical AI

Physical AI Application Domain



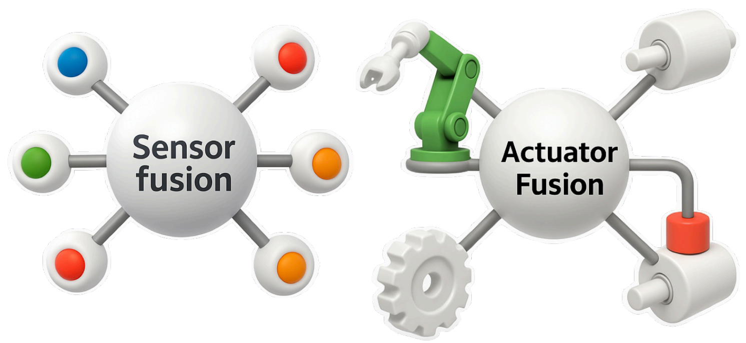

Physical AI Product Domain

Physical AI Control and Systems Domain

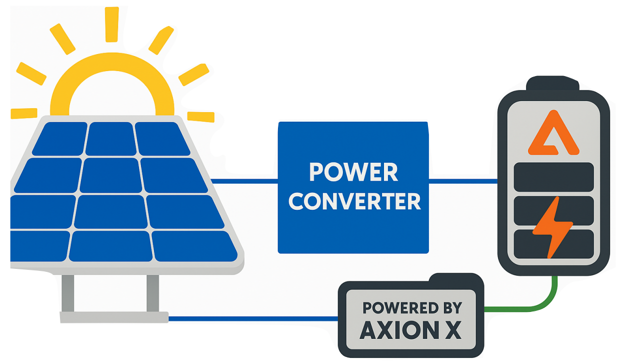
MI


MO

MIMO systems control



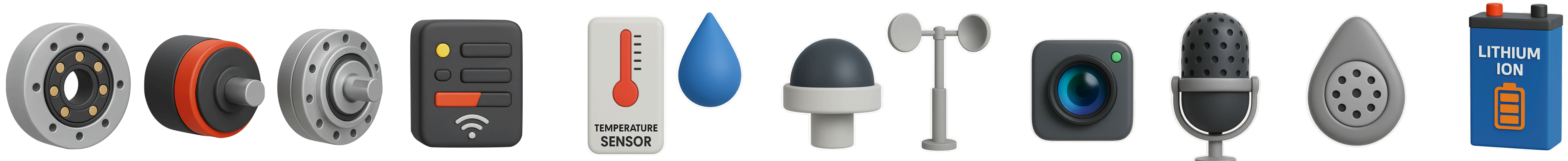
Sensor and Actuator Fusion



Energy harvesting

Electrification

Component Domain



Torque sensors | Servo motors | Harmonic Drives | Controllers | Temperature and humidity sensors | Light sensors | Wind sensors | Vison sensors | Sound sensors | Gas sensors | Batteries

Axion Cell/DFM

Specification → Architecture → HDL Design → Synthesis → Physical Design → Fabrication

Physical Design: Axion Cell, Axion DFM

Physical AI Open Platforms

- NVIDIA Omniverse
  - An open, real-time, physically accurate simulation and collaboration platform built on Universal Scene Description (USD)
  - Unifies AI, simulation, and digital-twin workflows across robotics, manufacturing, and industrial design
  - As an open platform, connects diverse tools, data, and developers into a scalable environment for creating intelligent, physics-based virtual worlds

- NVIDIA Omniverse provides the core, tools, and SDK, forming an open ecosystem platform

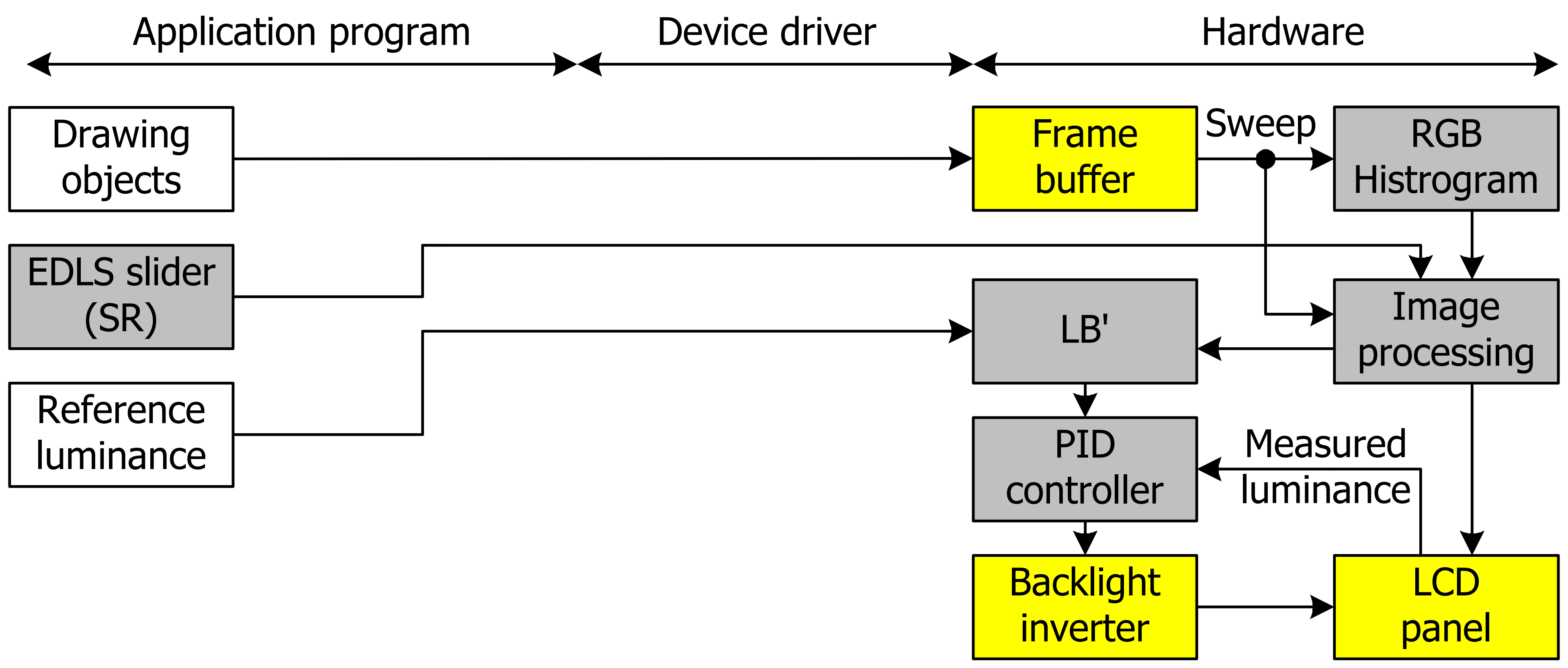
- Axion X supports assets with embedded domain knowledge (simulation models, simulation configurations, and AI training data)
  ↳ By leveraging physical systems, hardware, and controllers, Axion X enhances the capability for AI policy development, and further activates the overall Physical AI platform ecosystem

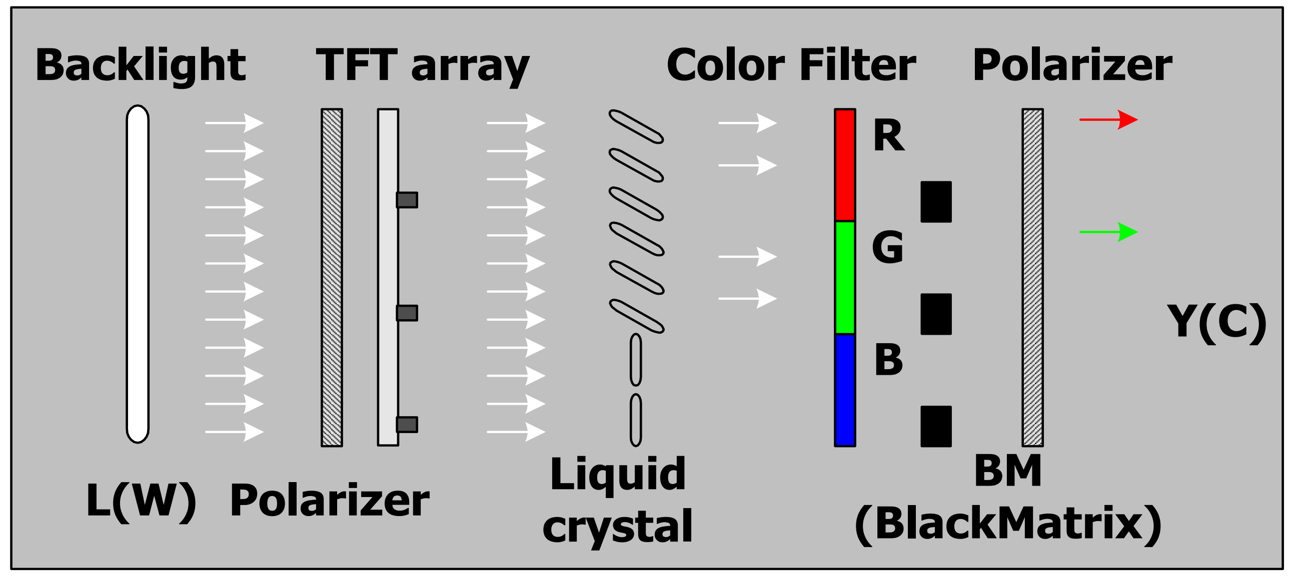
Open Platform

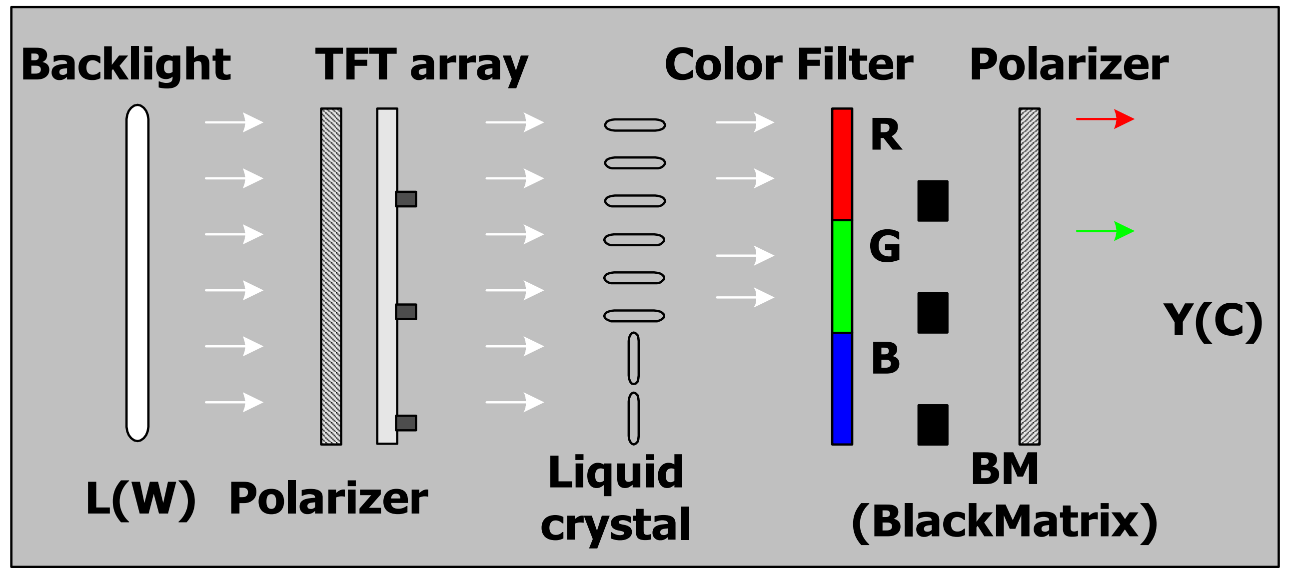
- Provides open interfaces (APIs), data, software, and partial hardware schematics so that external developers and third parties can freely access and use the platform
- The platform does not provide complete solutions, but rather offers common infrastructure (API, SDK, etc.)
- Users or external developers can build their own services on top of the platform
- Designed so that each user can customize, develop, and optimize based on their own objectives.

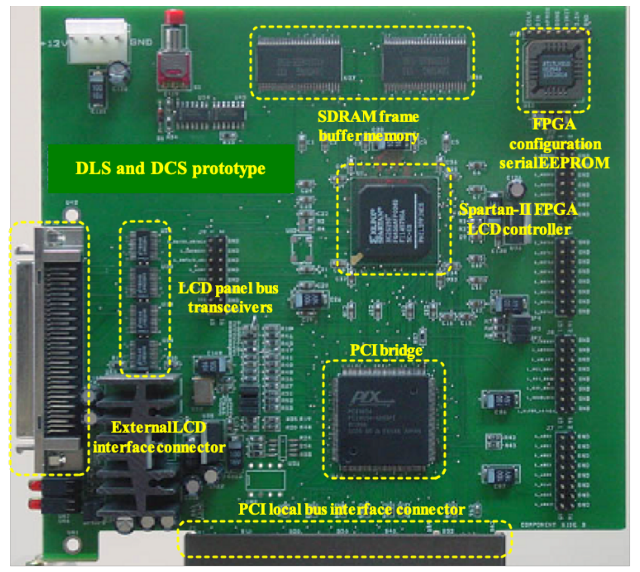
Physical AI PPA

- What is low-power LCD controller IP?
  - LCD controller chip consumes lower power
  - LCD controller may consume slightly more power internally, but it significantly reduces the total display power
    - Optimizing panel drive timing, refresh rates, and backlight duty → achieving net power savings at the system level.
- What is then PPA of AI robots?
  - For AI-driven robotic systems, PPA (Power, Performance, and Area) must be redefined holistically → beyond the silicon level.
- Physical AI PPA represents the holistic optimization of an entire embodied intelligent system → not just the AI chip or software model
  - Holistic Objective: Achieve globally optimal efficiency across sensors, compute, and actuators.
  - End-to-End Learning: Joint optimization of perception, control, and energy efficiency through data-driven training loops (simulation + real-world feedback)
  - Domain Knowledge Integration: Incorporate physical constraints, control theory, and material properties into AI models to ensure feasible and safe operation









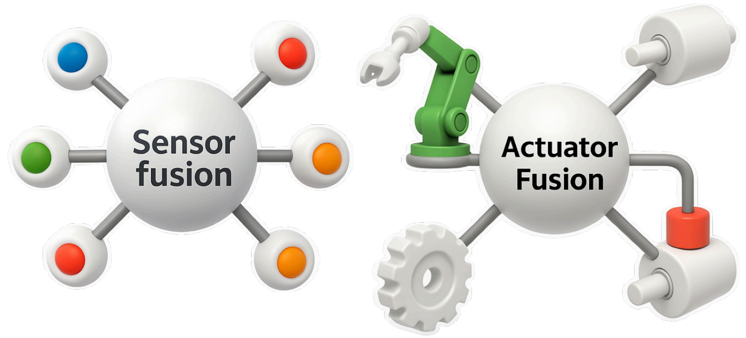
Domain Knowledge Encapsulation

- Bridging the gap between control and systems domains through integrated Physical AI policy development
- Encapsulating domain knowledge into pretrained, reusable AI libraries for scalable deployment
- Enabling PPA enhancement via end-to-end learning across design, control, and physical systems

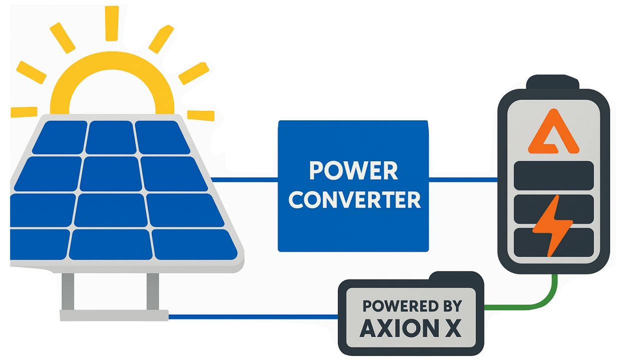
Physical AI Control and Systems Domain

MI  MO

MIMO systems control



Sensor and Actuator Fusion



Energy harvesting

Electrification

Physical AI

Domain Knowledge (control & systems)

- Specialized knowledge in specific domains
  - ↳ Vision and perception algorithms
  - ↳ Robot motion control theory
  - ↳ Classical control technologies
  - ↳ Position and attitude control method

Encapsulated into Axion X Physical AI Asset Library

Axion X Physical AI Library

Physical AI Assets

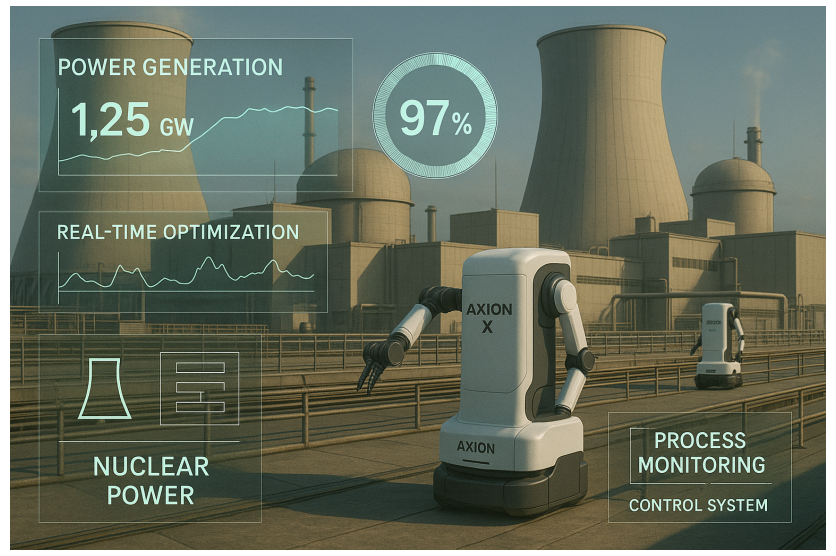
Physical AI open platforms

Design (simulation and policy) ⟷ Domain knowledge ⟷ Assets (AI models)

Physical AI user domains

Axion X opportunities

Physical AI Environment



End-to-end Learning (Full AI Design)

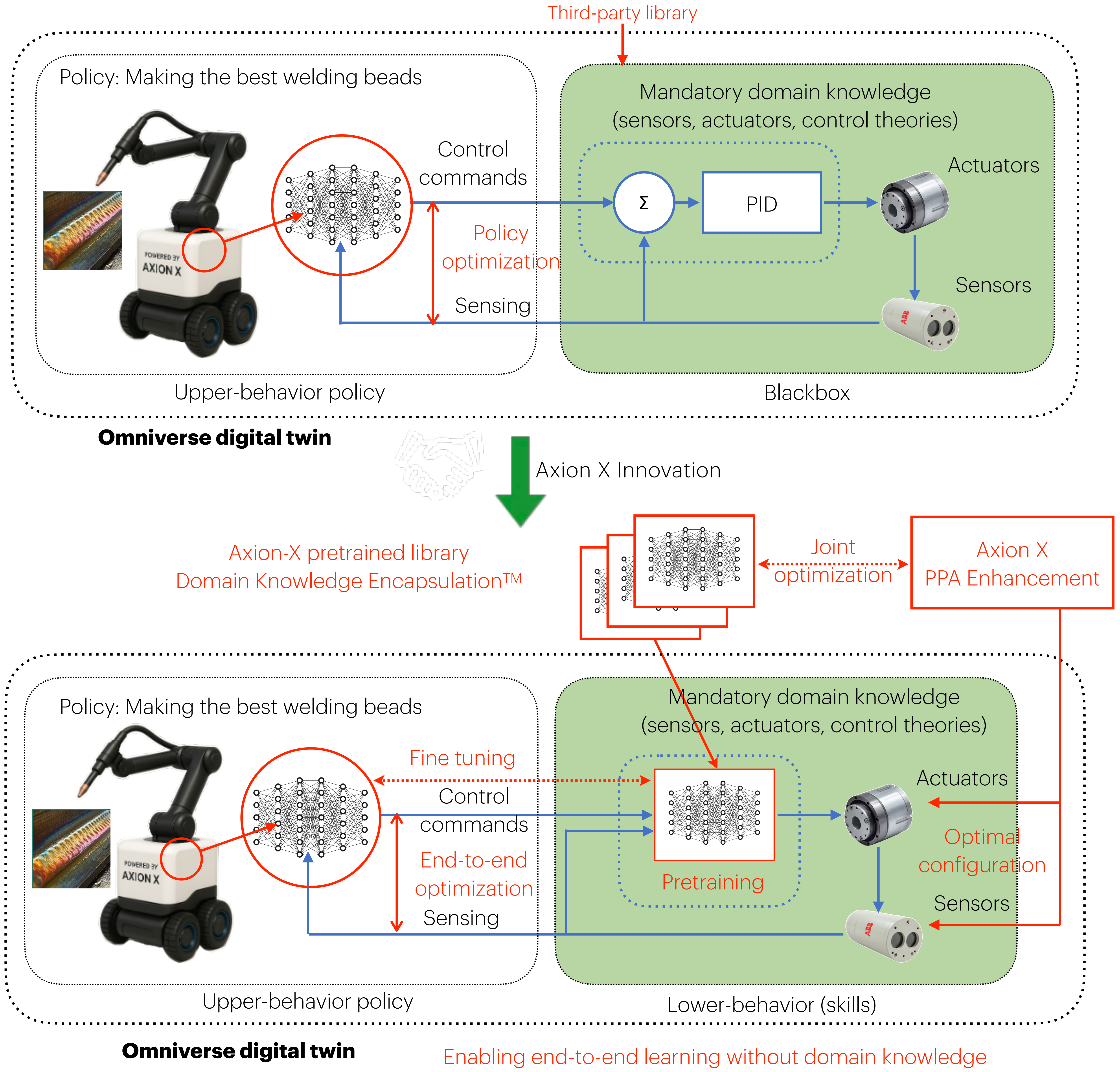
Physical AI PPA Enhancement

- P (Performance): Productivity, Quality
- P (Power): Energy Efficiency (OPEX)
- A (Area): Device Size / Cost (CAFEX)

Pretrained Physical AI Libraries

- Domain Knowledge Encapsulation™
  - ↳Originates from Axion Cell library optimization, control-system expertise, and DAoT (Design Automation of Things) principles
  - ↳Defines PPA (Performance, Power, Area) metrics as optimization indicators specific to Physical AI
  - ↳ Provides a unified optimization package solution by introducing co-design concepts that integrate hardware (PPA) and control systems, along with customizable reward-function design for application-specific optimization
  - ↳Enables Physical AI integrated optimization (Full AI Design), allowing AI engineers to focus on high-level policy development rather than low-level system tuning
  - ↳Supports end-to-end learning, enabling AI engineers to achieve continuous PPA improvement even without explicit system-domain knowledge

By encapsulating domain knowledge into reusable Physical AI Assets, Axion X enables scalable, end-to-end optimization of policy, perception, and control across physical domains, improving PPA metrics and accelerating deployment without requiring expert-level system knowledge



Attention-Based MIMO Control

- *Context-Aware* Sensor Fusion
  - ↳Conventional: Improves measurement accuracy by combining readings from multiple sensors
  - ↳Paradigm Shift: Integrates heterogeneous sensor data to model cross-sensor relationships and infer comprehensive environmental dynamics within a unified representation
- *Consequence-Aware* Actuator Fusion
  - ↳Paradigm Shift: Coordinates multiple actuators with overlapping dynamics to model cross-actuator interactions and infer their combined influence on the physical environment within a unified control framework.
- Aixon X MIMO control
  - ↳ Decomposes a complex MIMO control problem into multiple SISO control loops through context-aware sensor and consequence-aware actuator fusion, while maintaining overall system stability using conventional feedback control structures

Axion X Domain Knowledge Encapsulation™ AI Technology

✓ Sensor Feature Extraction using CNN: Extracts spatial and temporal variation patterns from multi-sensor data streams.

✓ Sensor Fusion via Attention: Achieves holistic situational awareness by learning cross-sensor dependencies and contextual correlations.

✓ Actuator Fusion via Attention: Interprets and coordinates environmental effects resulting from coupled or overlapping actuator behaviors.

✓ Optimal AI-based MPC (Model Predictive Control): Realizes model-based predictive control through reinforcement learning–driven optimization, integrating multi-sensor perception and multi-actuator control for adaptive system performance.

Conventional Temperature Control

Conventional SISO Temperature Control

✓ The temperature sensor detects a rise in room temperature

✓ The air conditioner is activated to lower the temperature

✓ The target temperature is maintained once equilibrium is reached

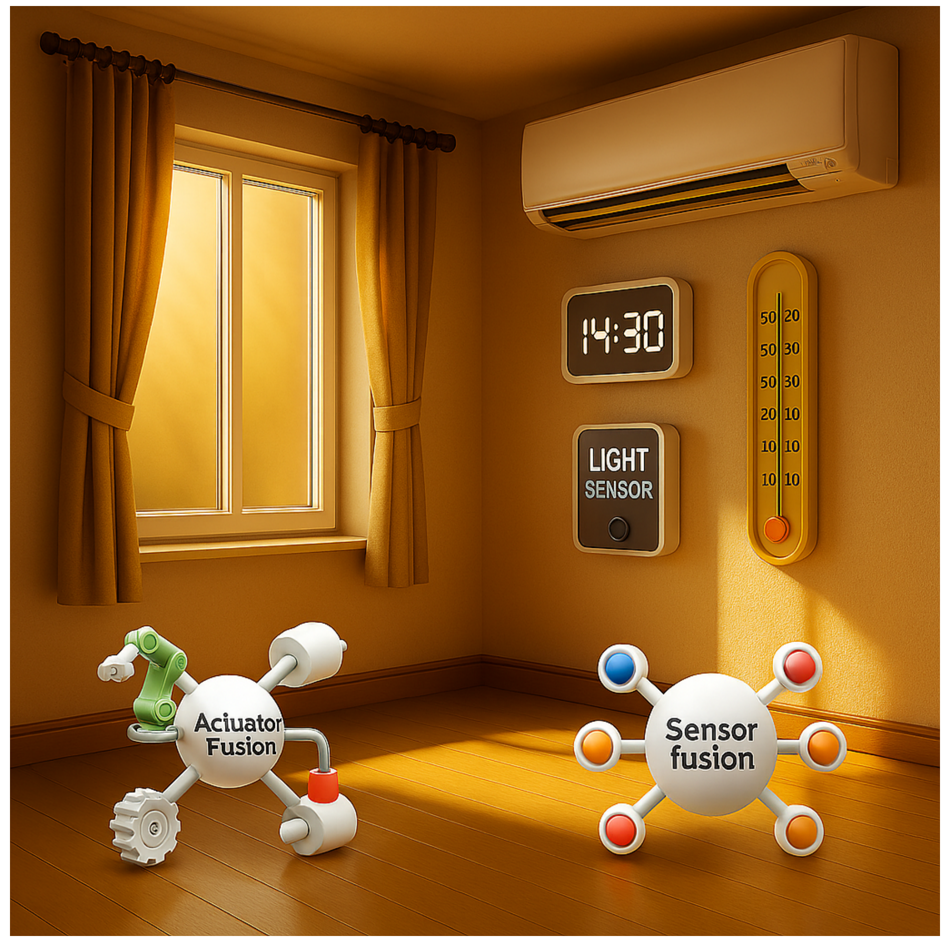
Axion X MIMO Temperature Control

Temperature sensor detects a rise in room temperature

Sensor fusion: Integrates data from temperature, illuminance, and time sensors to infer that the temperature increase is caused by a change in the sun's position

Actuator fusion: Coordinates multiple actuators to efficiently reduce the temperature: first closing the curtain to block sunlight, then activating the air conditioner fan

Maintains the target temperature economically and adaptively through coordinated sensor and actuator fusion



Remarks

- Axion has specialty in library-based design in semiconductor
- AI-based optimization
  - Netlist optimization
  - Layout optimization
  - LLM advisor
- Physical AI challenges
  - Lack of domain knowledge (more AI-oriented policy development engineers)
  - Control and systems domain expertise
  - Library-based design and optimization
  - Pretrained library with Domain Knowledge Encapsulation™
- My lifetime goal
  - To build and sustain a collaborative culture that achieves genuine, chemistry-level integration between Electrical Engineering and Computer Science
  - Why chemistry mixing?
  - Is CS and EE interface a border city or a PN junction?